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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,827	07/10/2001	Eric Mathew Trehus	2705-165	9201

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/902,827	TREHUS ET AL.	
	Examiner	Art Unit	
	Yolanda Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

SECOND DETAILED ACTION NON-FINAL

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,4,5,6,7,8,9,11 are rejected under 35 U.S.C. 102(e) as being anticipated by Marisetty et al. (USPN 6675324B2). As appears in claim 1, Marisetty et al. discloses a set of at least two masters; at least one target; at least one bus providing connection between the masters and the target; a system controller operable to determine if an error message is one that triggers quiesce and quiesce masters other than a master that received the error message from the set of masters if quiesce is triggered and a system error processor operable to handle an error condition indicated by the error message in column 8, line 65 – column 9, line 17 and column 5, lines 30-53.

3. As per claim 4, Marisetty et al. discloses wherein at least one bus includes a peripheral component interconnect bus in column 9, lines 7-8.

4. As per claim 5, Marisetty et al. discloses wherein the error message causing the system controller to quiesce the selected masters is programmable in column 5, lines 30-53.

5. As per claim 6, Marisetty et al. discloses at least one means for receiving and providing data; a set of means for addressing the means for receiving and providing data; a means for providing connection between the set of means for receiving and providing data and the at least one means for addressing; a means for determining if an error message is one that triggers quiesce and quiescing masters other than a master that received the error message form the set of masters if quiesce is triggers; and a means for handling an error condition indicated by the error message in column 8, line 65 – column 9, line 17 and column 5, lines 30-53.

6. As per claim 7, Marisetty et al. discloses wherein the error message causing the system controller to quiesce the selected masters may be programmable in column 5, lines 30-53.

7. As per claim 8, Marisetty et al. discloses receiving an error message indicating an error condition has arisen; determining if the error message is one which triggers auto quiesce; and generating auto quiesce signals to stop operations in the selected masters in column 5, lines 30-53.

8. As per claim 9, Marisetty et al. discloses wherein the method further comprises re-enabling the selected masters after the error condition has been cleared in column 8, lines 6-13.

9. As per claim 11, Marisetty et al. discloses wherein determining if the error message further is one which triggers auto quiesce further comprises preconfiguring a system controller with the error message in column 5, lines 30-53.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty et al. in view of Armany et al. (USPN 6412027B1). Marisetty et al. fails to explicitly state the set of masters includes at least one direct memory access controller.

Armany et al. discloses the function of a DMA controller in column 1, lines 36-40, "As computing systems advanced, DMA controllers were created to facilitate such data transfers by controlling the movement of data directly from one memory device to another memory device."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of masters includes at least one direct memory access controller. A person of ordinary skill in the art would have been motivated to have the set of masters includes at least one direct memory access controller because DMA controllers are used to control the transfer of data from one device to another device.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty et al. in view of Potter (USPN 5608884A). As per claim 3, Marisetty et al. fails to

explicitly state the set of masters includes at least one peripheral component interconnect controller.

Potter discloses a PCI controller in column 2, lines 38-39, "Also residing on the local bus 15 is a peripheral connection interface (or "PCI") controller..."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the set of masters includes at least one peripheral component interconnect controller. A person of ordinary skill in the art would have been motivated to have the set of masters includes at least one peripheral component interconnect controller because the PCI controller is used to control signals between devices on different buses. Potter discloses in column 2, lines 39-43, "(or "PCI") controller 18 which controls exchanges of address, data and control signals between devices residing on the local bus 15, for example, the CPU 14, and devices residing on a PCI bus 20 coupled to the local bus 15 by a bridge 22."

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty et al. in view of Berg et al. (USPN 6629184). As per claim 10, Marisetty et al. fails to explicitly state the error message is an interrupt.

Berg et al. discloses in column 9, lines 55-60, "hard disk drive 20 immediately determines that 01h is an invalid command, and in response to this determination, generates an interrupt by asserting line INTRQ, and generates and error message by setting ERR in the status register and ABRT in the error register."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the error message be an interrupt. A person of

ordinary skill in the art would have been motivated to have the error message be an interrupt because interrupts indicate that an error has occurred in the computer system. Berg et al. discloses in column 9, lines 60-64, "CPU 10 responds to the interrupt by reading the status register and detecting that ERR is set and then responds to ERR being set by reading the error register and detecting that ABRT is set. In this fashion, CPU 10 is informed that the write operation has not occurred."

14. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Marisetty et al. in view of Yazdy (USPN 5815676). Marisetty et al. fails to explicitly state signaling an address arbiter to halt address grants for the selected masters.

Yazdy discloses signaling an address arbiter to halt address grants for the selected masters in column 3, lines 60-67 – column 4, lines 1-2, "Exemplary embodiments of the present invention provide an address arbiter which handles split bus transactions... In addition to prioritizing requests from those bus masters, the address arbiter also handles two cases where the arbiter prevents any of the bus masters from acquiring the address bus."

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have an address arbiter to halt address grants for the selected masters. A person of ordinary skill in the art would have been motivated to store the solution to have an address arbiter to halt address grants for the selected masters because address arbiters are used to handle which devices can or cannot have access to an address bus.

Response to Arguments

15. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection. The addition of new subject matter into independent claims 1 and 6 caused the previous rejection to be changed. Arguments pertaining to the prior art, Natsume et al., used in the first office action are moot in view of the use of new prior art, Marisetty et al., used in the rejection as indicated above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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